We claim:

1. An electronic component with shielding against stray electromagnetic fields, the electronic component comprising:

a ground potential terminal for receiving an external ground potential;

a semiconductor chip having a semiconductor substrate with an active upper side and a passive rear side having a surface area;

at least one ground lead disposed within said semiconductor substrate;

a buried layer being electrically conductive and having a surface area corresponding in size to said surface area of said passive rear side, said buried layer disposed within said semiconductor substrate in a region of said passive rear side and connected to said ground potential terminal through said ground lead; and

at least one contact area disposed on said upper side of said semiconductor substrate.

2. The electronic component according to claim 1, wherein said buried layer is formed of a semiconductor material doped with an impurity concentration of over 1×10^{20} cm^{-3}.

3. The electronic component according to claim 2, wherein said semiconductor material is identical to a material forming said semiconductor substrate.

4. The electronic component according to claim 1, wherein said semiconductor substrate is formed of monocrystalline silicon.

5. The electronic component according to claim 1, including an electrically conductive annular layer extending from said upper side of said semiconductor substrate to said buried layer, and disposed in an edge region of said semiconductor chip.

6. The electronic component according to claim 5, wherein said electrically conductive annular layer is formed of a semiconductor material doped with an impurity concentration of over 1×10^{20} cm^{-3}.

7. The electronic component according to claim 1, wherein the electronic component is a component of a flip-chip mounting technique.

8. The electronic component according to claim 1, wherein the electronic component is a radio-frequency component.

9. The electronic component according to claim 1, including solder formations selected from the group consisting of solder balls and solder contact bumps disposed on said contact area.

10. The electronic component according to claim 9, including a mounting device selected from the group consisting of a printed circuit board and a ceramic substrate, and said solder formations mounted to said mounting device.

11. The electronic component according to claim 5, including:

output contact areas;

a wiring foil with connecting lines disposed on said upper side of said semiconductor substrate, said contact area of said semiconductor chip is one of a plurality of contact areas and said connecting lines of said wiring foil connecting said contact area of said semiconductor chip to said output contact areas distributed on said wiring foil; and

solder formation selected from the group consisting of solder balls and solder contact bumps disposed on said output contact areas.

12. The electronic component according to claim 11, wherein said ground potential terminal is connected through at least one of said solder formations, through said wiring foil and through said annular layer to said buried layer.

13. A method for producing an electronic component with shielding, which comprises the steps of:

providing a semiconductor wafer functioning as a semiconductor substrate formed of a semiconductor material and having an active upper side for at least one integrated circuit and a passive rear side;

implanting impurities from the passive rear side of the semiconductor wafer for forming a buried layer being electrically conductive and having a surface area corresponding in size to a surface area of the passive rear side of the semiconductor substrate;

introducing an electrically conductive annular layer from the active upper side of the semiconductor wafer as far as the buried layer in an edge region of the integrated circuit;

producing the integrated circuit within the electrically conductive annular layer in the semiconductor substrate defining a semiconductor chip; and

packaging the semiconductor chip to form the electronic component with the shielding.

14. The method according to claim 13, which comprises doping the semiconductor material with an impurity concentration of at least 1×10^{20} cm^{-3} for producing the buried layer.

15. The method according to claim 14, which comprises forming and soldering solder formations selected from the group consisting of solder balls and solder contact bumps onto contact areas on the active upper side of the semiconductor wafer.

16. The method according to claim 15, which comprises connecting the solder formations to a support selected from the group consisting of a printed-circuit board and a ceramic substrate, and connecting at the same time at least one of the solder formations to a ground potential terminal.

17. The method according to claim 15, which comprises connecting the contact areas to connecting lines of a wiring foil having further solder formations selected from the group consisting of solder balls and solder contact bumps.

18. The method according to claim 17, which comprises connecting the further solder formations of the wiring foil to lines of a support selected from the group consisting of a printed-circuit board and of a ceramic substrate, at least one of the further solder formations being connected to a ground-carrying line of the support.

19. The method according to claim 13, which comprises disposing an annular contact area, which establishes electrical contact with the electrically conductive annular layer, in an edge region of the upper side of the semiconductor chip.

20. The method according to claim 18, which comprises electrically connecting one of a number of annularly disposed solder balls and a number of annularly disposed solder contact bumps to the electrically conductive annular layer in an edge region of the individual semiconductor chip.

21. A method for producing an electronic component with shielding, which comprises the following steps:

providing a semiconductor wafer functioning as a semiconductor substrate having an active upper side for at least one integrated component and a passive rear side;

growing an electrically conductive layer formed of an electrically conductive semiconductor material and thereafter an electrically intrinsically conductive layer formed of an electrically intrinsic conductive semiconductor material on the active upper side of the semiconductor wafer by epitaxial growth, the electrically conductive layer becoming a buried layer adjacent the electrically intrinsically conductive layer;

introducing an electrically conductive annular layer from the active upper side of the semiconductor wafer, the electrically conductive annular layer extending through the electrically intrinsically conductive layer as far as the buried layer, the electrically conductive annular layer disposed in an edge region of the semiconductor substrate;

producing the integrated circuit within the electrically conductive annular layer in the semiconductor substrate defining a semiconductor chip; and

packaging the individual conductor chips to form the electronic component with the shielding.

22. The method according to claim 21, which comprises doping the semiconductor material with an impurity concentration of at least 1×10^{20} cm^{-3} for forming the buried layer.

23. The method according to claim 22, which comprises forming and soldering solder formations selected from the group consisting of solder balls and solder contact bumps onto contact areas on the active upper side of the semiconductor wafer.

24. The method according to claim 23, which comprises connecting the solder formations to a support selected from the group consisting of a printed-circuit board and a ceramic substrate, and connecting at the same time at least one of the solder formations to a ground potential terminal.

25. The method according to claim 23, which comprises connecting the contact areas to connecting lines of a wiring foil, the wiring foil having further solder formations selected from the group consisting of solder balls and solder contact bumps.

26. The method according to claim 25, which comprises connecting the further solder formations of the wiring foil to lines of a support selected from the group consisting of a printed-circuit board and of a ceramic substrate, at least one of the further solder formations being connected to a ground-carrying line of the support.

27. The method according to claim 21, which comprises disposing an annular contact area, which establishes electrical contact for the electrically conductive annular layer, in an edge region of the upper side of the semiconductor chip.

28. The method according to claim 26, which comprises electrically connecting one of a number of annularly disposed solder balls and a number of annularly disposed solder contact bumps to the electrically conductive annular layer in an edge region of the semiconductor chip.